

AN11003 Pegoda Amplifier

Pegoda Amplifier

Rev. 1.0 — 3 November 2010

Application note

Document information

Info	Content
Keywords	RFID, Antenna Design, RF Amplifier, Antenna Matching, contactless reader
Abstract	This application note provides guidance on antenna and RF amplifier design for NXP Pegoda reader device.



Revision history

Rev	Date	Description
1.0	20101104	Initial Release

Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

1.1 Purpose and Scope

Some of NXP contactless reader IC's are designed for handheld devices and low power consumption which results in shorter read range performance. An RF amplifier can extend the usage of such devices to meet requirements for higher transmission performance and communication distance.

This application note is intended to give a practical guide to extend and optimize the transmission power performance and communication distance of Pegoda reader IC's based on RC523 and RX852. The document describes the design and dimension of antennas and RF amplifier circuits.

1.2 Referenced documents

1. ISO/IEC 14443

For information on availability of samples as well as documentation, please refer to the application note 'Pegoda EV710/EV852 Documentation and Sampling guide'.

1.3 Referenced Simulation Tools

1. RFSim99

2. How to use this document

The application note gives a practical guide to design antennas, calculate the matching components as well as implement an RF amplifier for NXP contactless reader IC RC523 and RX852. It gives a guideline for complete RF circuit design as well as a description of the transmitter matching resistance. Finally the matching procedure is described using a reference antenna which is connected to the amplifier circuit.

A guideline is given to design an antenna and the RF amplifier circuitry together with a tuning procedure. The guideline covers the following items:

2. RF field generation and data transmission
 - a. Fig 1 shows the recommended amplifier circuit with all relevant components required to connect an antenna to NXP's contactless NFC reader IC's. This circuit must not only ensure that energy and data can be transmitted to the target device but must also be designed to receive a target device's answer.
 - b. The antenna design part describes how to calculate the inductance of the antenna coil and gives basic hints on symmetry and environmental influences to be taken into consideration. The equivalent circuits and the relevant formulas are given as preparation for these calculations.
 - c. Formulas to calculate the amplifier and the matching circuit
 - d. Antenna tuning procedure
3. Receiver part
 - a. Design and calculation of the receiver circuit.
4. Examples on how to calculate the RF parts for a given antenna design and given contactless reader IC.

Note: This application note cannot and does not replace any of the relevant datasheets.

Note: The term "Card" used in this document refers to a contactless smart card according to the ISO14443 scheme.

Note: Design hints on how to place the components on a PCB are not included.

Note: All tuning and measurement of the antenna always has to be performed at the final mounting position to consider all parasitic effects like metal influence on quality factor, inductance and additional capacitance.

3. Block Diagram

The amplifier solution is designed to communicate in:

- Reader/Writer mode for communication with devices compliant to ISO/IEC14443A
- Reader/Writer mode for communication with devices compliant to ISO/IEC14443B is planned for future releases

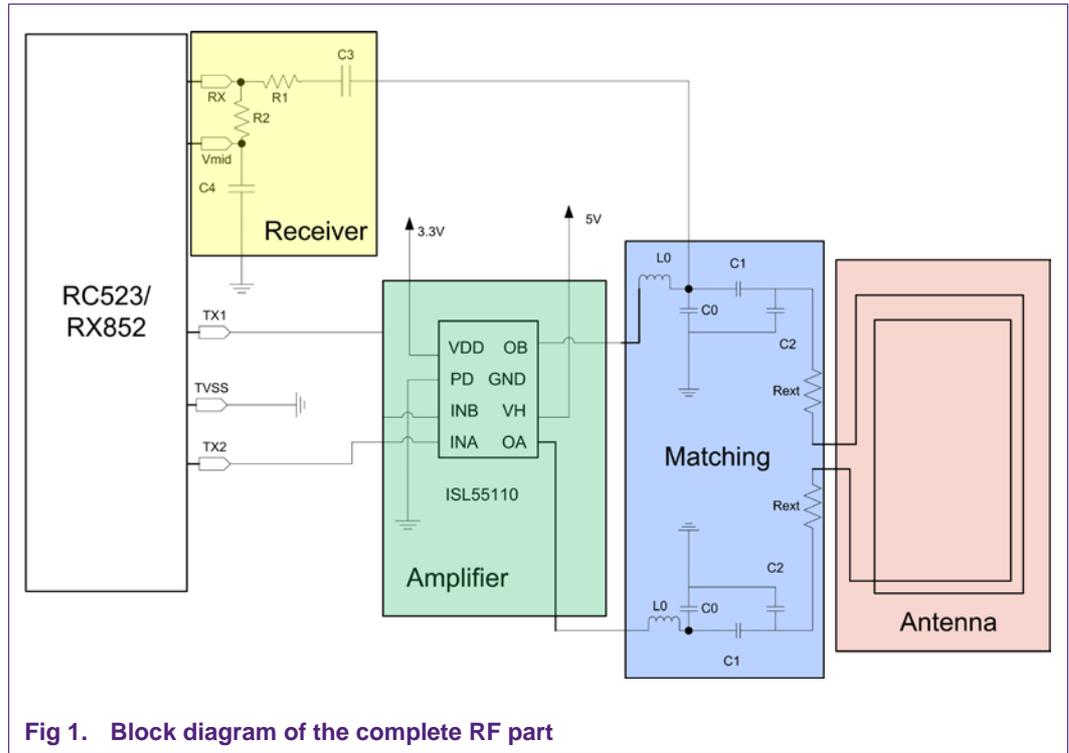
For an amplifier solution different to the presented MOSFET implementation please refer to AN1425xx

The following requirements have to be met by the amplifier circuit for NXP contactless reader:

- **Generate the RF field:** The generated magnetic field has to be maximized considering the limits of the transmitter supply current and general emission limits.
- **Transmit data:** The coded and modulated data signal has to be transmitted in a way, that every card is able to receive it. The signal shape and timing has to be considered.
- **Receive data:** The response of a card has to be transferred to the receive input of the reader IC considering the datasheet limits like maximum voltage and receiver sensitivity.

The operating distance of NXP contactless reader IC's depends on:

- matching of the antenna,
- sensitivity of the receiver,
- antenna size used in the reader system,
- antenna size of the communication partner and
- external parameters (e.g. metallic environment and noise).



Note: Fig 1 shows the RF part only. For proper operation, the analog and digital supplies plus the host interface also have to be connected to power supply.

Although some of these blocks may contain only a few passive components, it is important to consider all blocks and complete functionality to guarantee proper function of the complete device:

- The amplifier uses a mosfet switch to amplify the digital signal of the NXP contactless reader IC.
- The matching circuit acts as an impedance transformation block.
- The EMC filter as part of the matching circuit reduces the 13.56 MHz harmonics and performs an impedance transformation.
- The antenna coil itself generates the magnetic field.
- The receiver part provides the received signal to the NXP contactless reader internal receiver stage.

Note: A center tap connection of the antenna may be neglected without negative influence on the EMC performance of the circuitry.

4. Description of Symmetric Amplifier

The colored boxes as well as the schematic in Fig 1 show the different parts of the circuit. Each box will be separately discussed in the following chapters.

4.1 Amplifier Circuit

The Amplifier Circuit (TX-Path) (green box in Fig 1) consists of a high speed mosfet pair acting as a switch. The TX1 and the TX2 output of the NXP contactless reader chip generates a digital signal which is amplified by the FET structure. The signal is directly connected to the matching circuit.

4.2 Antenna Matching

Depending on the antenna PCB (red box in Fig 1), the necessary antenna matching (blue box Fig 1) consists of a symmetric arrangement of an EMC – filter (L0 and C0) plus a serial and parallel tuning capacitors, from the reader chip point of view. To regulate the quality factor of the antenna, the resistor R_q is added.

The capacitors and the resistors are used to both achieve the required 13.56MHz resonance frequency, and a quality factor for appropriate signal shaping according to ISO/IEC 14443.

The following equations in chapter 4.3 are used to calculate the matching components. Please keep in mind, that these values, slightly modified, are also required for fine tuning the components. This is necessary because of the direct influence of the amplifier circuit onto the phase shifting of the two signals on both sides of the antenna matching circuit. The maximum output is reached when the antenna is first tuned to 13.56MHz and the two ends of the antenna tuning circuit, connected to the amplifier, oscillate (in relation to GND) with 180 degree phase shift.

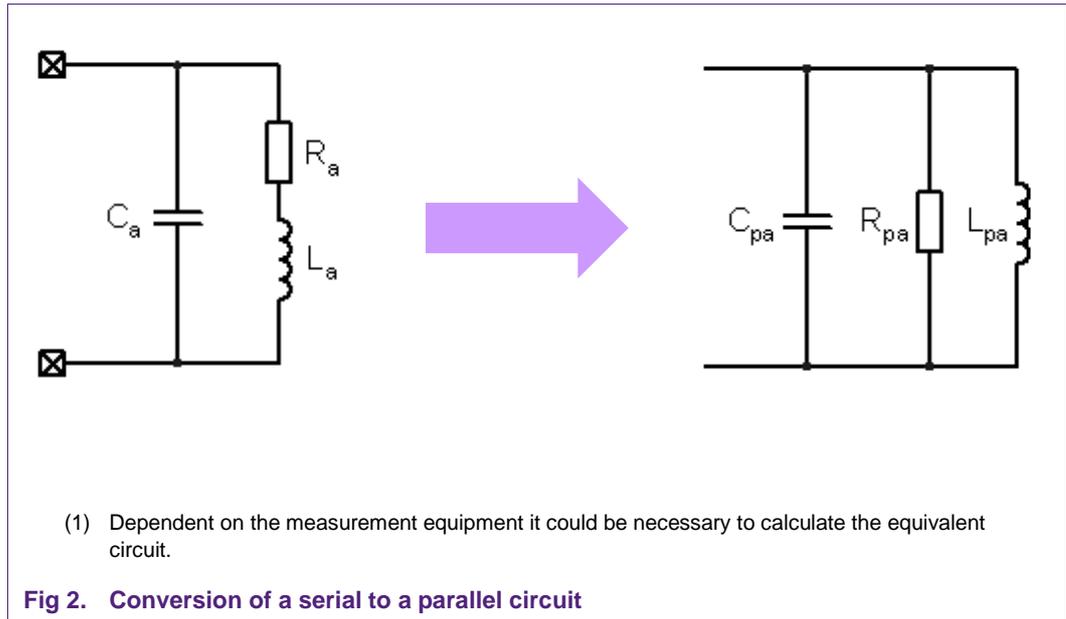
The electrical parameters of the antenna L_p , R_p and C_p have to be measured first.

Note: The matching of the antenna is very strong influenced by its environment. An assembled PCB or other metallic environment, like a display or housing will make a retuning necessary.

4.3 Mathematical Deduction

4.3.1 Calculation of the Equivalent circuit with the focus on the quality factor

Measuring the antenna by using a network analyzer or a RFA-Bridge, gives the inductance (L_a), the serial resistor (R_a), as well as the natural frequency (f_{nat}). To calculate the tuning capacitors, the components for the equivalent parallel circuit have to be calculated first.



The adjustment of the quality factor for the antenna has to be done during the calculation of the equivalent circuit. This is accomplished by adding ohmic resistance, which changes the R_{sges} . (Refer to Table 1 and chapter 6)

Table 1. Mathematical deduction to calculate the equivalent circuit

Step	Equation	Comment
1. Calculation of the R_{sges}	$Q = \frac{\omega L_{pa}}{R_{sges}}$	L_{pa} ...Measured ω for 13.56MHz Q...chosen
2. Out of R_{sges} one can calculate R_{pa}	$R_{pa} = \frac{(\omega L_{pa})^2}{R_{sges}}$	L_{pa} ...done R_{pa} ...done
3. Calculation of C_{pa}	$f_{nat} = \frac{1}{2\pi\sqrt{(L_{pa} \cdot C_{pa})}}$	f_{nat} ... Mearsured L_{pa} ...Measured C_{pa} ...done

4.3.1.1 Calculation of the tuning capacitors

Due to the filter structure, it is necessary to split the circuit to calculate the tuning capacitors. $R_{match} = Z_{match} = 50 \text{ Ohm}$

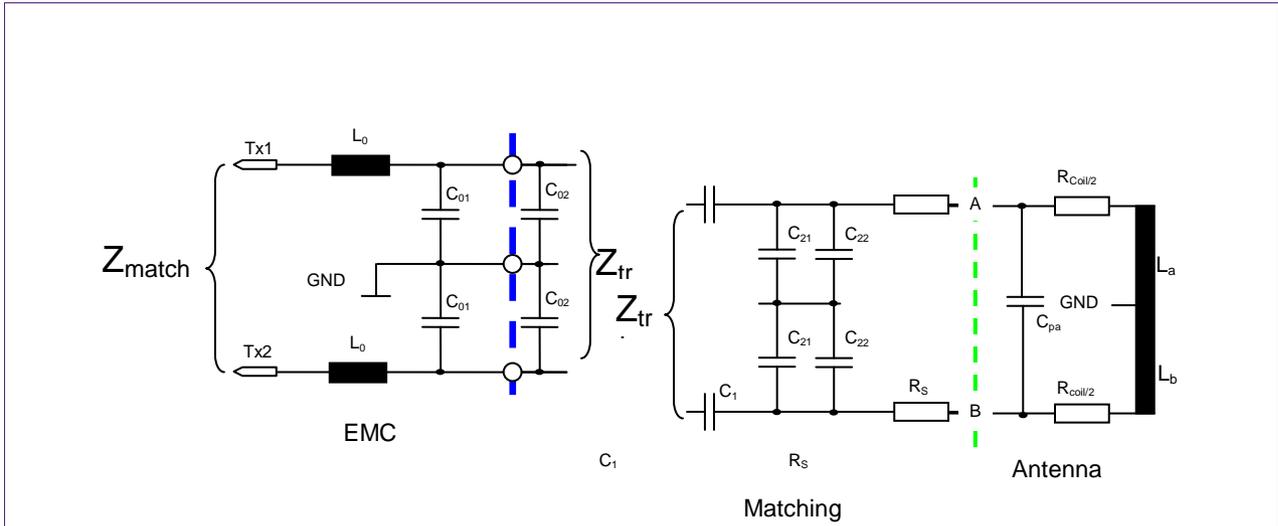


Fig 3. Split of the matching circuit because of the filter structure

$$Z_{tr} = R_{tr} + jX_{tr}$$

$$R_{tr} = \frac{R_{match}}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2}$$

$$X_{tr} = 2 \cdot \omega \cdot \frac{L_0 \cdot \left(1 - \omega^2 \cdot L_0 \cdot C_0\right) - \frac{R_{match}^2}{4} \cdot C_0}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2}$$

Fig 4. Equations to calculate the tuning capacitors (part 1)

The split of the matching circuit allows calculating the matching capacitors with following equations.

$$C_1 \approx \frac{1}{\omega \cdot \left(\sqrt{\frac{R_{tr} \cdot R_{pa}}{4}} + \frac{X_{tr}}{2} \right)}$$

$$C_2 \approx \frac{1}{\omega^2 \cdot \frac{L_{pa}}{2}} - \frac{1}{\omega \cdot \sqrt{\frac{R_{tr} \cdot R_{pa}}{4}}} - 2 \cdot C_{pa}$$

Fig 5. Equations for the calculation of the tuning capacitors (part 2)

Note: For calculating the tuning capacities NXP provides an Excel sheet [1] where all this calculations are done automatically.

4.3.2 Receive Path

The receiver path (yellow box at Fig 1) consists of a voltage divider and two capacitors. The capacitor C_3 is necessary to decouple DC voltage and the following resistor R_3 limits the voltage to prevent clipping at the $R_x -$ pin of the NXP contactless reader IC.

To guarantee a well tuned receiver circuit, one needs to consider both: the voltage level and also the receive threshold. Refer also to the data sheet of the contactless reader IC.

5. Antenna Design

5.1 Antenna Inductance

The following two sections show the formulas to estimate the antenna inductance in free air.

To estimate antenna values under influence of metal (such as shielding planes or batteries in devices) simulation software is required which can calculate the antennas parameters in these environments.

5.1.1 Circular Antennas

The inductance can be estimated by the following formula (see also Fig 6):

$$L_a [nH] = \frac{24.6 \cdot N_a^2 \cdot D [cm]}{1 + 2.75 \cdot \frac{s [cm]}{D [cm]}} \quad (1)$$

D Average antenna diameter

s Antenna width

N_a Number of turns

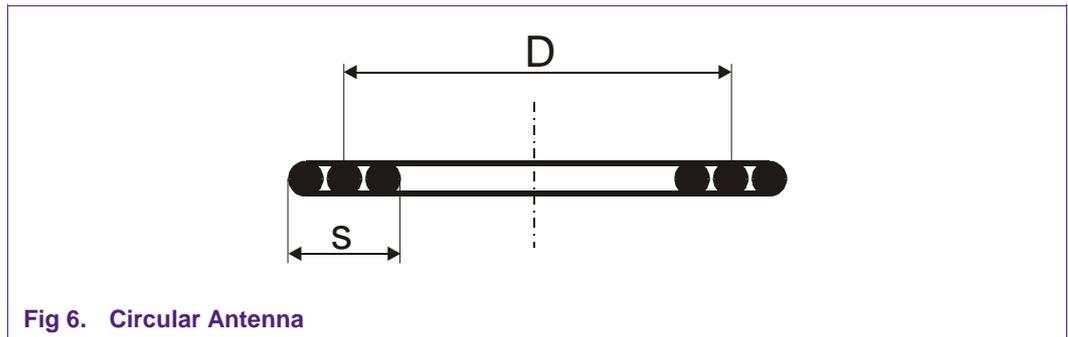


Fig 6. Circular Antenna

5.1.2 Rectangular Antennas

The inductance can be calculated by following formula (see also Fig 7):

$$L_a = \frac{\mu_0}{\pi} \cdot [x_1 + x_2 - x_3 + x_4] \cdot N_a^{1.8} \quad (2)$$

Table 2. Calculations for rectangular antenna

With:

$$d = \frac{2 \cdot (t + w)}{\pi}$$

$$a_{avg} = a_o - N_a \cdot (g + w)$$

$$b_{avg} = b_o - N_a \cdot (g + w)$$

$$x_1 = a_{avg} \cdot \ln \left[\frac{2 \cdot a_{avg} \cdot b_{avg}}{d \cdot (a_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2})} \right] \quad x_2 = b_{avg} \cdot \ln \left[\frac{2 \cdot a_{avg} \cdot b_{avg}}{d \cdot (b_{avg} + \sqrt{a_{avg}^2 + b_{avg}^2})} \right]$$

$$x_3 = 2 \cdot \left[a_{avg} + b_{avg} - \sqrt{a_{avg}^2 + b_{avg}^2} \right]$$

$$x_4 = \frac{a_{avg} + b_{avg}}{4}$$

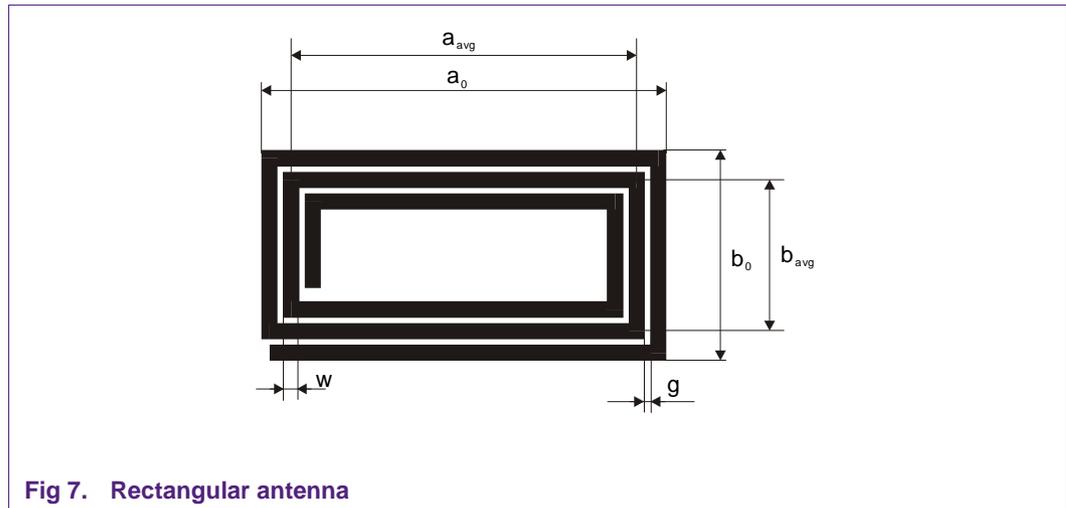


Fig 7. Rectangular antenna

Variables:

- a_o, b_o Overall dimensions of the coil
- a_{avg}, b_{avg} Average dimensions of the coil
- t Track thickness
- w Track width
- g Gap between tracks
- N_a Number of turns
- d Equivalent diameter of the track

5.2 Number of Turns

Depending on the antenna size, the number of turns should be chosen in a way to achieve an antenna inductance between 300 nH and 3 μ H.

The parasitic capacitance should be kept as low to achieve a self-resonance frequency > 35 MHz.

For many applications and antenna sizes, the number of turns will be in the range **$N_a = 1 - 6$** .

A low number of turns is preferred to minimize the effects of coupling between antennas. The lower the numbers of turns are used, the smaller will be the influence of coupled devices. It is especially important to minimize the detuning effect on the 1st device in very close proximity between the antennas where this coupling has maximum impact. The overall performance loss due to low number of turns is negligible.

5.3 Antenna Quality Factor

The quality factor reflects the stored energy in the antenna. When the Q – factor is high the antenna needs more time to react on modulation, but radiates more energy. This directly influences the shaping of the radiated and modulated signal and the operating volume.

The bandwidth B –pulse width multiplied by T is defined as:

$$B \cdot T \geq 1 \quad (3)$$

With the bandwidth definition

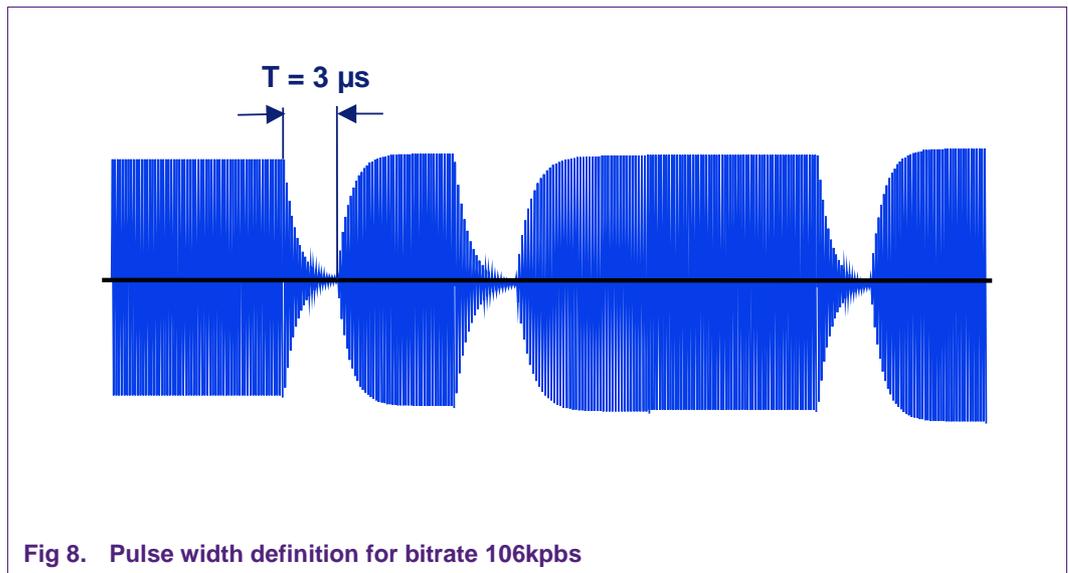
$$B = \frac{f}{Q} \quad (4)$$

B multiplied by T results into

$$Q \leq f \cdot T$$

$$Q \leq 13.56 \text{ MHz} \cdot 3 \mu\text{s}$$

$$Q \leq 40.68$$



The recommended antenna quality factor to be used is $Q_a \leq 30$ for data rates up to 106kpbs. For higher data rates a lower Q factor of below 20 is recommended.

In general, a lower quality factor improves the stability of communication in terms of antenna detuning and faster signal transitions. The consequence of lower quality factors results in reduced output power and read range.

6. Implementation Guideline

This chapter explains a step by step process to design and tune the amplifier circuit.

6.1 Antenna and tuning circuit

The example uses an antenna PCB with the size of 84 mm x 64 mm and 2 turns.

6.1.1 Measurement of the Antenna

Measure the inductance L_{pa} , the serial resistance R_s and the self-resonance frequency f_{nat} of the antenna with a network analyzer or equivalent equipment.

The example antenna has following values:

Table 3. Measured Values of Sample Antenna

Antenna	Value
L_{pa}	811nH
$R_{sAntenna}$	370mΩ
f_{nat} (of the Antenna)	89.7MHz

6.1.2 Calculation of the Resistance of the Equivalent Circuit

Calculation of the additional resistor R_{ext} , for a quality factor of 25 (refer to Table 1: Mathematical deduction to calculate the equivalent circuit).

A quality factor of 25 was chosen to guarantee the needed shaping for the modulation.

$$R_{sges} = \frac{\omega L_{pa}}{Q} = \frac{2 * \pi * 13.56MHz * 811nH}{25} = 2.76Ohm$$

$$R_{ext} = \frac{R_{sges} - R_{sAntenna}}{2} = \frac{2.76Ohm - 0.37Ohm}{2} = 1.2Ohm$$

Table 4. Description of the ohmic resistors for the sample antenna

Name	Description
$R_{sAntenna}$	Ohmic resistance of the Antenna; measured
R_{ext}	Additional calculated resistors needed to reach the quality factor Q of 25
R_{sges}	Complete resistance consist of the $R_{sAntenna} + 2 * R_{ext}$

6.1.3 Calculate out of R_{sges} the equivalent R_{pa}

$$R_{pa} = \frac{(\omega L_{pa})^2}{R_{sges}} = \frac{(2 * \pi * 13.56MHz * 811nH)^2}{2.76Ohm} = 1.73kOhm$$

6.1.4 Calculation of the Parallel Capacity of the Antenna.

$$C_{pa} = \frac{1}{\omega_{nat}^2 L_{pa}} = \frac{1}{(2 * \pi * 89,7MHz)^2 * 811nH} = 3.88pF$$

Note: The capacitance is a behavior of the antenna and is calculated using the measured inductance and “natural frequency” of the antenna.

6.1.5 Calculation of the tuning Capacitances

$$C1 = \frac{1}{\omega \cdot \sqrt{\frac{R_{tr} \cdot R_{pa}}{4} + \frac{X_{tr}}{2}}} \approx 42pF$$

$$C2 = \frac{1}{\omega^2 \cdot \frac{L_{pa}}{2}} - \frac{1}{\omega \sqrt{\frac{R_{tr} \cdot R_{pa}}{4}}} - 2 \cdot C_{pa} \approx 290pF$$

Note: NXP provides an Excel sheet [1] to calculate the tuning capacitors

6.1.5.1 Simulation

The simulation shows the arrangement of the matching circuit plus its smith chart

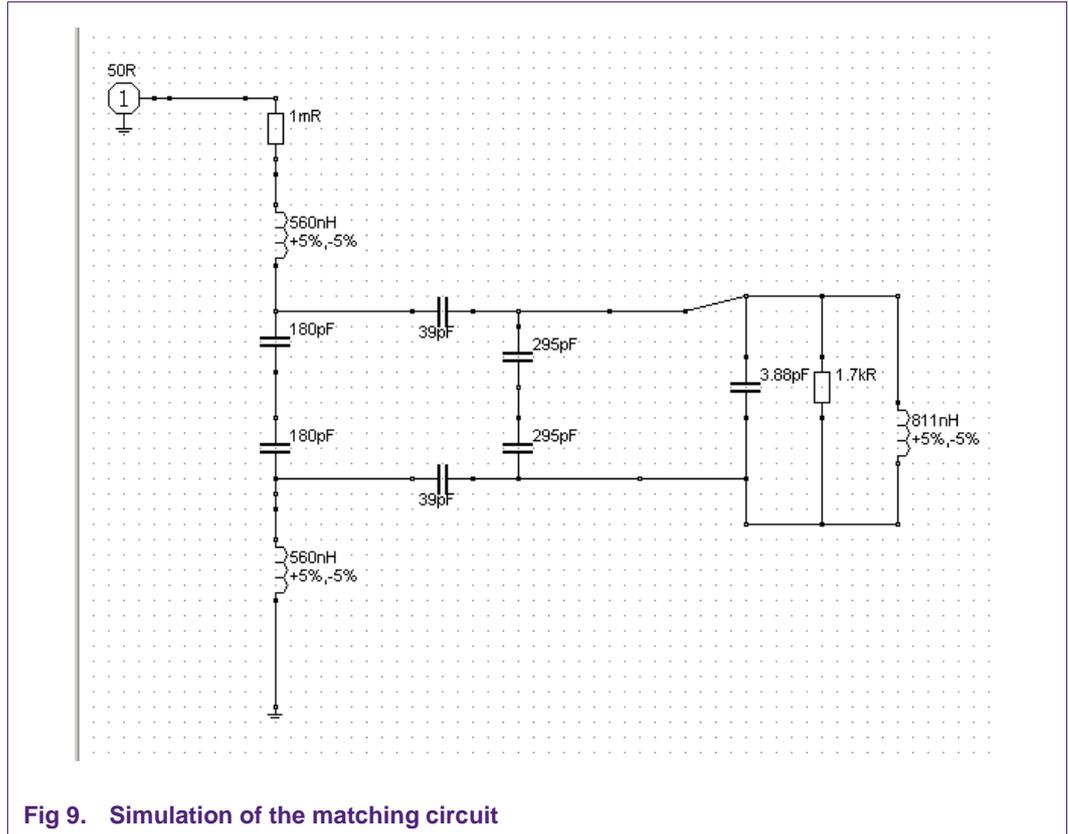


Fig 9. Simulation of the matching circuit

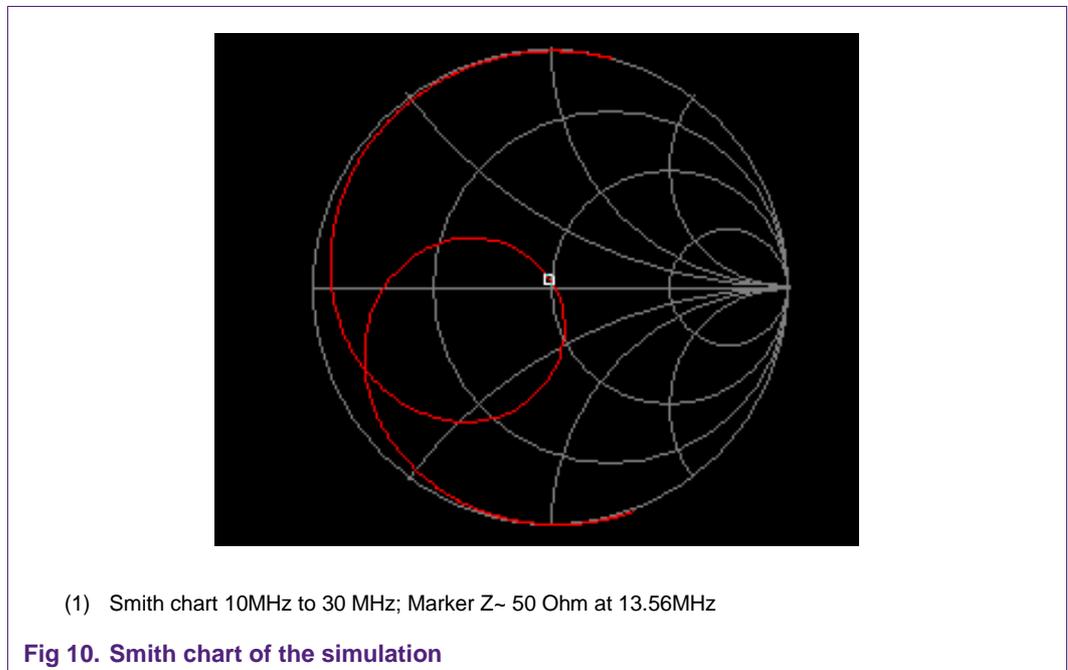


Fig 10. Smith chart of the simulation

Table 5. Values of the Tuning Circuit

Component	Value
R_{ext}	1.20hm
C1	39pF
C2	295pF
C0	180pF
L0	560nH

6.2 Receive Path

C₃ decouples the DC-voltage. The resistors R₁ and R₂ limit the voltage to prevent clipping at the Rx – pin of the NXP contactless reader IC.

Note: The voltage at R_x should never be higher than 3 V_{pp} (measured with a low capacitance probe). Increase the resistor R₁ if the voltage is too high.

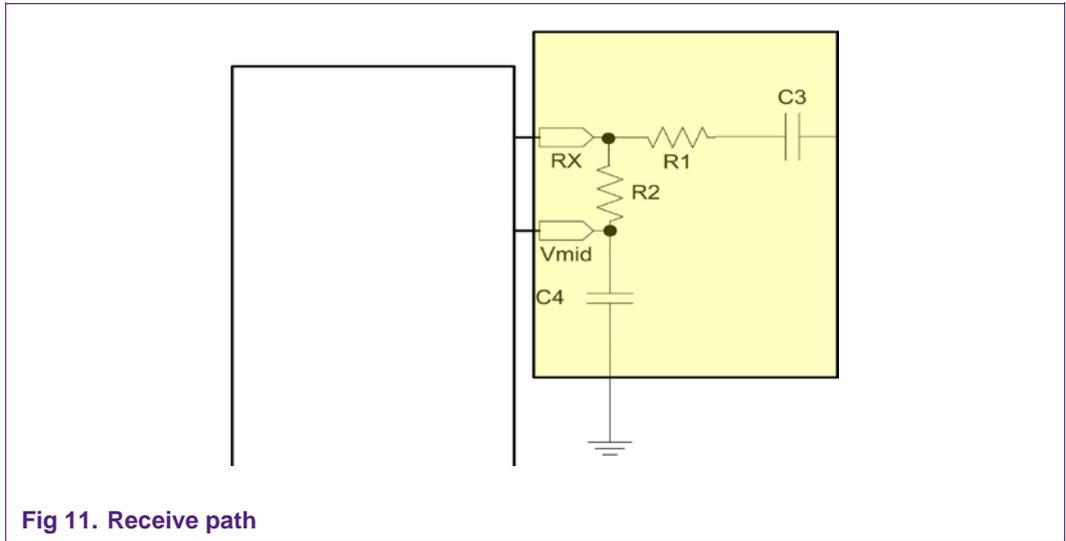


Fig 11. Receive path

Table 6. Example values of the Receive Path

Components for receive filter	Values
R ₁	3.3kOhm
R ₂	1kOhm
C ₃	1nF
C ₄	100nF

6.3 Summary

6.3.1 Component list

The bill of material for the Pegoda amplifier components and the full circuit can be found in the corresponding excel sheet as well in the schematics contained in the package.

7. Fine Tuning

A well matched antenna can be achieved by fine tuning the circuit. The adjustments needed to be done are based on the receiving and matching block.

- The resistor R_1 in the receiving path, in combination with R_2 , is a voltage divider which regulates the voltage level at the R_x pin. The voltage level should not exceed $3 V_{pp}$, but should be maximized for optimum R/W performance. The measurement of the voltage level at the R_x pin needs to be done with a low capacitance probe. Furthermore, those measurements needs to be done in the final housing/position as well as with different loads (targets) which detune the antenna and affects the RX signaling.
- In order to optimize the antenna tuning bring the antenna into its final housing/position and tune the antenna by changing C_1 , C_2 and C_0 . The optimum matching impedance for the antenna differ from design to design, but should be in the range of $Z=50 \pm j0$ (@ 13.56 MHz).

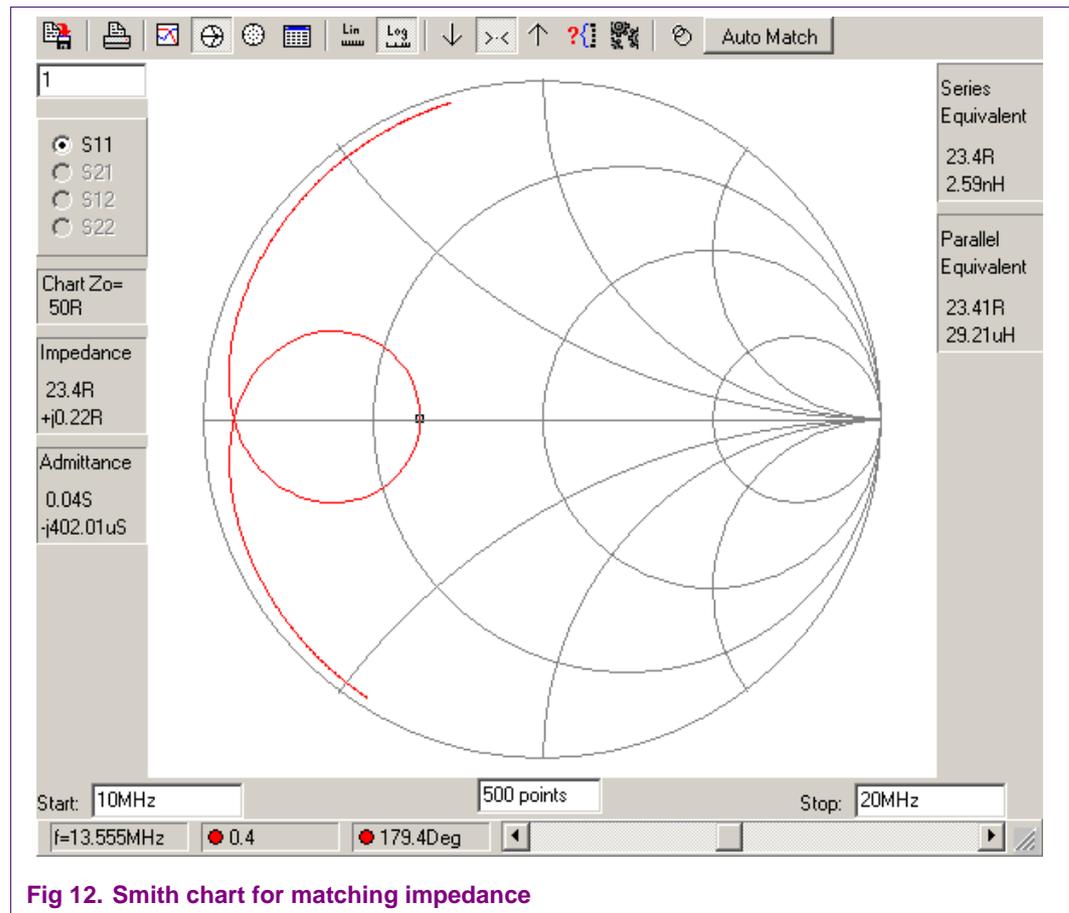
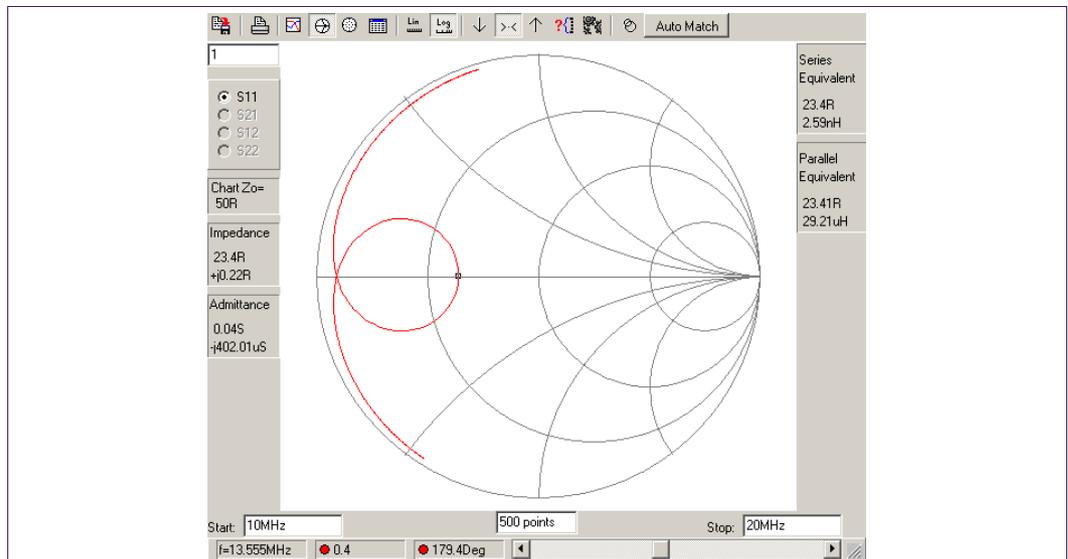


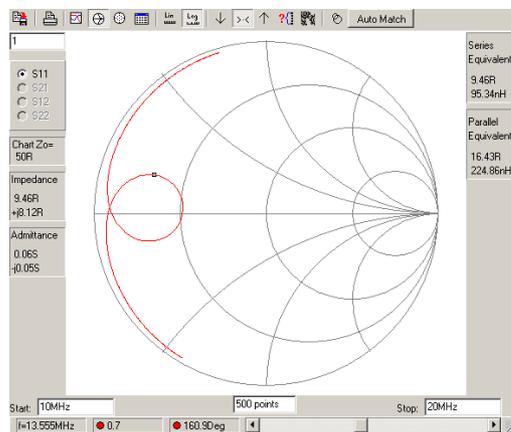
Fig 12. Smith chart for matching impedance

7.1 Tuning of series matching capacitance C_1

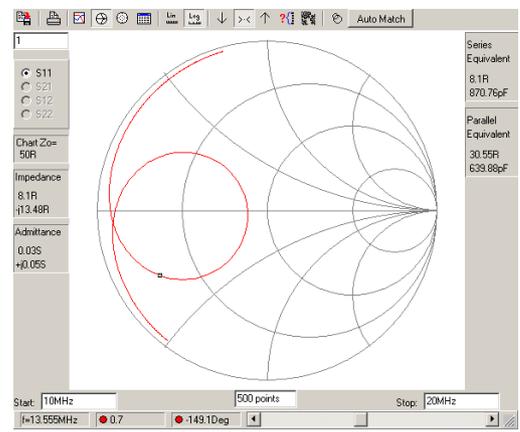
The Smith charts show the matching impedance $Z_{match} / 2$ vs. frequency. This means the plots show half of the antenna circuit, instead of 50Ohm for the full circuit, only 25Ohms are seen on one side of the antenna matching circuit.



a. Optimum C_1



b. C_1 too low



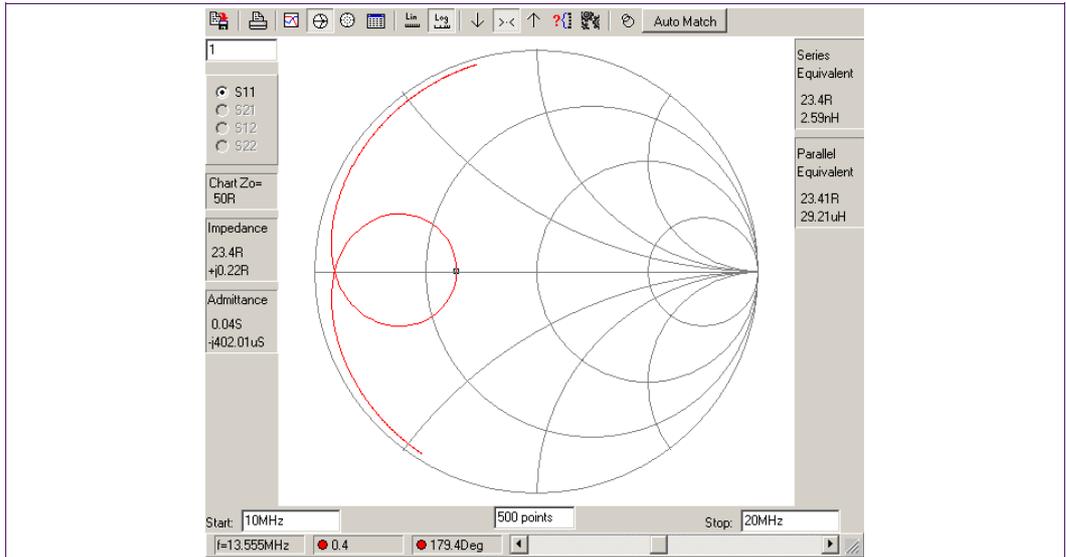
c. C_1 too high

Fig 13. Smith charts for C_1 tuning

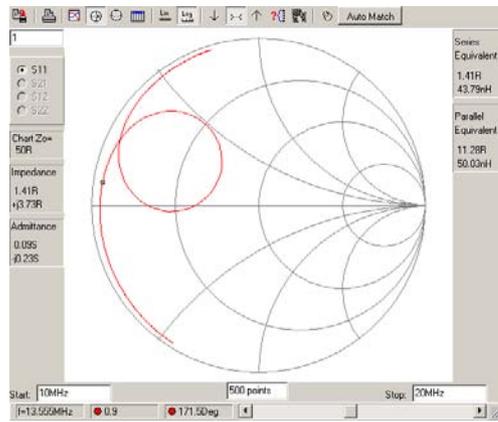
C_1 changes the magnitude of the matching impedance. After a change of C_1 the imaginary part of Z_{match} must be compensated by adjusting C_2 .

7.2 Tuning of parallel matching capacitance C_2

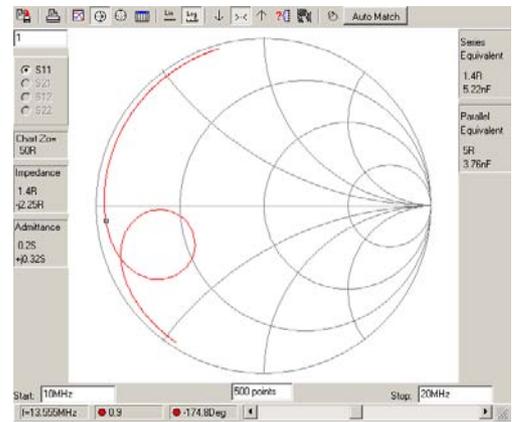
The smith charts show the matching impedance $Z_{match} / 2$ vs. frequency.



d. Optimum C_2



e. C_2 too low

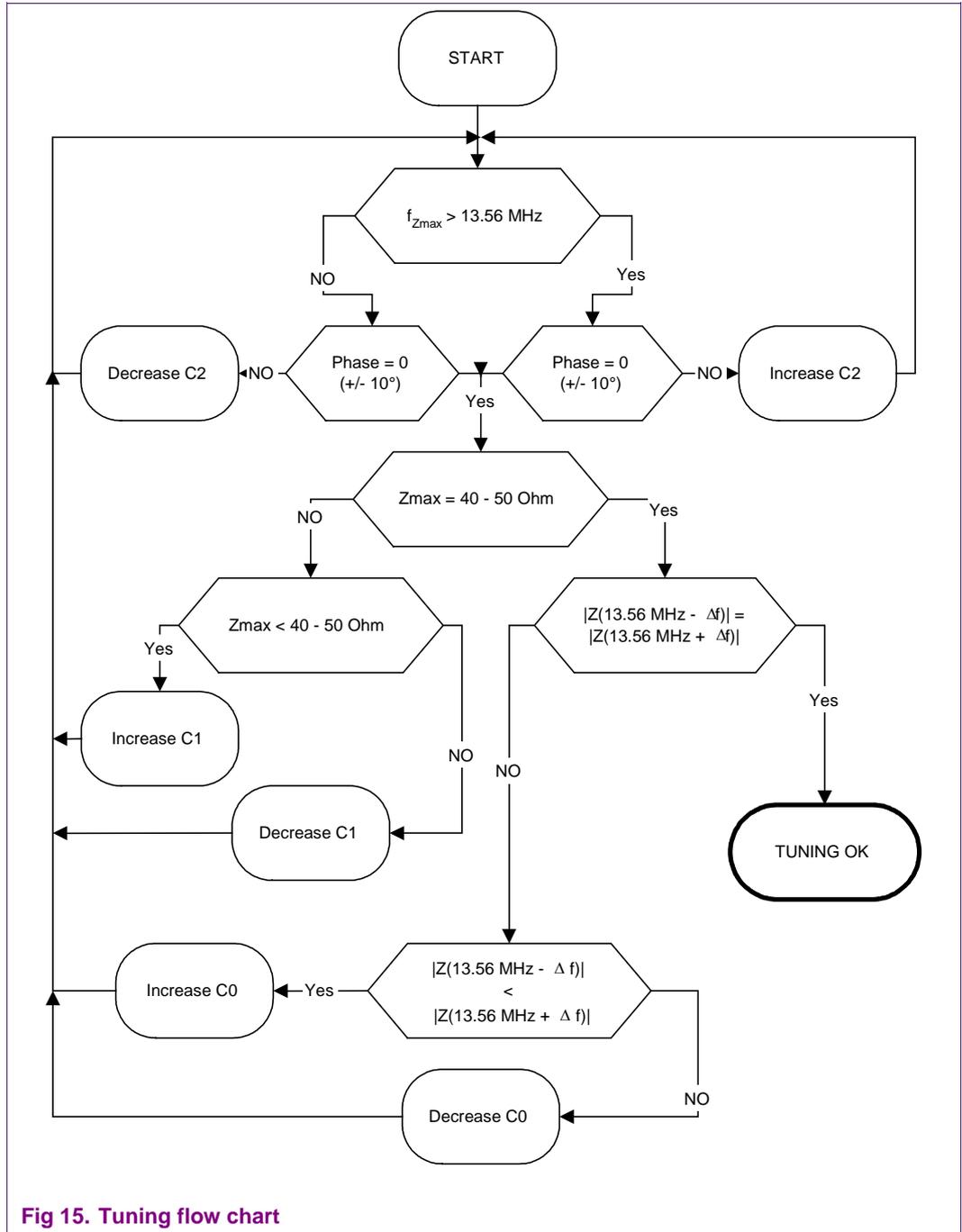


f. C_2 too high

Fig 14. Smith charts for C_2 tuning

C_2 changes mainly the imaginary part of Z_{match} .

7.3 Tuning Flow-Chart



8. Legal information

8.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and

the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

8.3 Licenses

Purchase of NXP ICs with ISO/IEC 14443 type B functionality



This NXP Semiconductors IC is ISO/IEC 14443 Type B software enabled and is licensed under Innovatron's Contactless Card patents license for ISO/IEC 14443 B.

The license includes the right to use the IC in systems and/or end-user equipment.

RATP/Innovatron Technology

8.4 Patents

Notice is herewith given that the subject device uses one or more of the following patents and that each of these patents may have corresponding patents in other jurisdictions.

<Patent ID> — owned by <Company name>

8.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

MIFARE — is a trademark of NXP B.V.

MIFARE Ultralight — is a trademark of NXP B.V.

MIFARE Plus — is a trademark of NXP B.V.

9. List of figures

Fig 1. Block diagram of the complete RF part.....6

Fig 2. Conversion of a serial to a parallel circuit8

Fig 3. Split of the matching circuit because of the filter structure.....9

Fig 4. Equations to calculate the tuning capacitors (part 1)9

Fig 5. Equations for the calculation of the tuning capacitors (part 2) 10

Fig 6. Circular Antenna 11

Fig 7. Rectangular antenna..... 12

Fig 8. Pulse width definition for bitrate 106kpbs..... 14

Fig 9. Simulation of the matching circuit 17

Fig 10. Smith chart of the simulation..... 17

Fig 11. Receive path..... 19

Fig 12. Smith chart for matching impedance.....20

Fig 13. Smith charts for C₁ tuning.....21

Fig 14. Smith charts for C₂ tuning.....22

Fig 15. Tuning flow chart.....23

10. List of tables

- Table 1. Mathematical deduction to calculate the equivalent circuit 8
- Table 2. Calculations for rectangular antenna 12
- Table 3. Measured Values of Sample Antenna..... 15
- Table 4. Description of the ohmic resistors for the sample antenna..... 15
- Table 5. Values of the Tuning Circuit..... 18
- Table 6. Example values of the Receive Path 19

11. Contents

1.	Introduction	3	10.	List of tables	26
1.1	Purpose and Scope.....	3	11.	Contents	27
1.2	Referenced documents	3			
1.3	Referenced Simulation Tools	3			
2.	How to use this document.....	4			
3.	Block Diagram	5			
4.	Description of Symmetric Amplifier	7			
4.1	Amplifier Circuit.....	7			
4.2	Antenna Matching	7			
4.3	Mathematical Deduction.....	7			
4.3.1	Calculation of the Equivalent circuit with the focus on the quality factor	7			
4.3.1.1	Calculation of the tuning capacitors	9			
4.3.2	Receive Path.....	10			
5.	Antenna Design	11			
5.1	Antenna Inductance	11			
5.1.1	Circular Antennas.....	11			
5.1.2	Rectangular Antennas.....	11			
5.2	Number of Turns	13			
5.3	Antenna Quality Factor	13			
6.	Implementation Guideline.....	15			
6.1	Antenna and tuning circuit.....	15			
6.1.1	Measurement of the Antenna	15			
6.1.2	Calculation of the Resistance of the Equivalent Circuit.....	15			
6.1.3	Calculate out of R_{sges} the equivalent R_{pa}	16			
6.1.4	Calculation of the Parallel Capacity of the Antenna.....	16			
6.1.5	Calculation of the tuning Capacitances	16			
6.1.5.1	Simulation	17			
6.2	Receive Path.....	19			
6.3	Summary.....	19			
6.3.1	Component list	19			
7.	Fine Tuning	20			
7.1	Tuning of series matching capacitance C_1	21			
7.2	Tuning of parallel matching capacitance C_2	22			
7.3	Tuning Flow-Chart.....	23			
8.	Legal information	24			
8.1	Definitions	24			
8.2	Disclaimers.....	24			
8.3	Licenses.....	24			
8.4	Patents.....	24			
8.5	Trademarks.....	24			
9.	List of figures.....	25			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.